

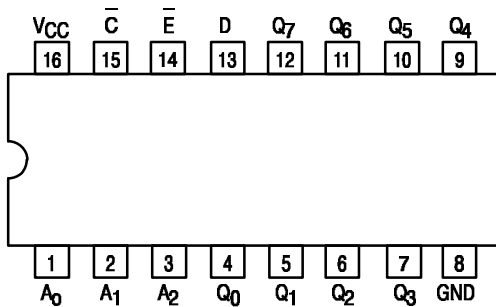


## 8-BIT ADDRESSABLE LATCH

The SN54/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

|                                                  |                                 |
|--------------------------------------------------|---------------------------------|
| A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | Address Inputs                  |
| D                                                | Data Input                      |
| $\bar{E}$                                        | Enable (Active LOW) Input       |
| $\bar{C}$                                        | Clear (Active LOW) input        |
| Q <sub>0</sub> to Q <sub>7</sub>                 | Parallel Latch Outputs (Note b) |

### LOADING (Note a)

|                                                  | HIGH     | LOW          |
|--------------------------------------------------|----------|--------------|
| A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> | 0.5 U.L. | 0.25 U.L.    |
| D                                                | 0.5 U.L. | 0.25 U.L.    |
| $\bar{E}$                                        | 1.0 U.L. | 0.5 U.L.     |
| $\bar{C}$                                        | 0.5 U.L. | 0.25 U.L.    |
| Q <sub>0</sub> to Q <sub>7</sub>                 | 10 U.L.  | 5 (2.5) U.L. |

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

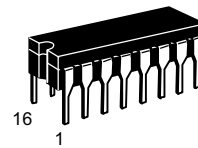
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### GUARANTEED OPERATING RANGES

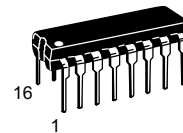
| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | -55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | -0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## SN54/74LS259

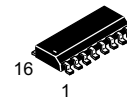
### 8-BIT ADDRESSABLE LATCH LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08



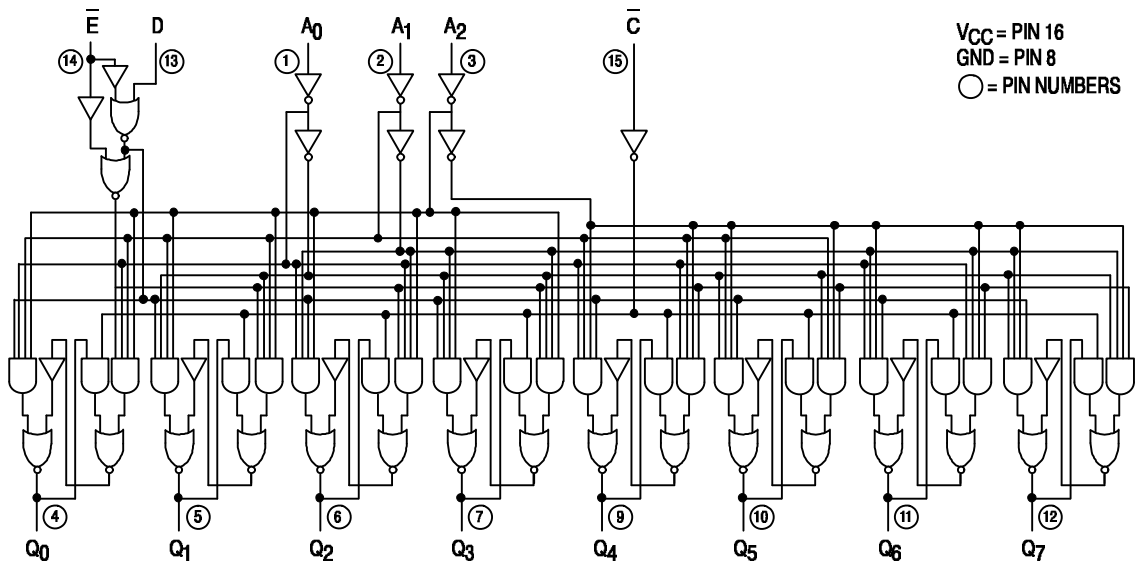
**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

|            |         |
|------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC    |

# SN54/74LS259

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The SN54/74LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the

addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the SN54/74LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The truth table below summarizes the operations.

## MODE SELECTION

| E | C | MODE                                    |
|---|---|-----------------------------------------|
| L | H | Addressable Latch                       |
| H | H | Memory                                  |
| L | L | Active HIGH Eight-Channel Demultiplexer |
| H | L | Clear                                   |

## TRUTH TABLE PRESENT OUTPUT STATES

| C | E | D | A <sub>0</sub> | A <sub>1</sub> | A <sub>2</sub> | Q <sub>0</sub>   | Q <sub>1</sub>   | Q <sub>2</sub>   | Q <sub>3</sub>   | Q <sub>4</sub>   | Q <sub>5</sub>   | Q <sub>6</sub>   | Q <sub>7</sub>   | MODE              |
|---|---|---|----------------|----------------|----------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|
| L | H | X | X              | X              | X              | L                | L                | L                | L                | L                | L                | L                | L                | Clear Demultiplex |
| L | L | L | L              | L              | L              | L                | L                | L                | L                | L                | L                | L                | L                |                   |
| L | L | H | L              | L              | L              | H                | L                | L                | L                | L                | L                | L                | L                |                   |
| L | L | L | H              | L              | L              | L                | L                | L                | L                | L                | L                | L                | L                |                   |
| L | L | H | H              | L              | L              | L                | H                | L                | L                | L                | L                | L                | L                |                   |
| L | L | H | H              | H              | H              | L                | L                | L                | L                | L                | L                | L                | H                |                   |
| H | H | X | X              | X              | X              | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Memory            |
| H | L | L | L              | L              | L              | L                | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Addressable Latch |
| H | L | H | L              | L              | L              | H                | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |
| H | L | L | H              | L              | L              | Q <sub>N-1</sub> | L                | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |
| H | L | H | H              | L              | L              | Q <sub>N-1</sub> | H                | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |
| L | L | L | L              | L              | L              | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |
| L | L | L | L              | L              | L              | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |
| H | L | L | H              | H              | H              | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Addressable Latch |
| H | L | H | H              | H              | H              | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> | Q <sub>N-1</sub> |                   |

X = Don't Care Condition  
L = LOW Voltage Level  
H = HIGH Voltage Level  
Q<sub>N-1</sub> = Previous Output State

# SN54/74LS259

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol   | Parameter                      |        | Limits |       |      | Unit          | Test Conditions                                                                                           |
|----------|--------------------------------|--------|--------|-------|------|---------------|-----------------------------------------------------------------------------------------------------------|
|          |                                |        | Min    | Typ   | Max  |               |                                                                                                           |
| $V_{IH}$ | Input HIGH Voltage             |        | 2.0    |       |      | V             | Guaranteed Input HIGH Voltage for All Inputs                                                              |
| $V_{IL}$ | Input LOW Voltage              | 54     |        |       | 0.7  | V             | Guaranteed Input LOW Voltage for All Inputs                                                               |
|          |                                | 74     |        |       | 0.8  |               |                                                                                                           |
| $V_{IK}$ | Input Clamp Diode Voltage      |        |        | -0.65 | -1.5 | V             | $V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$                                                         |
| $V_{OH}$ | Output HIGH Voltage            | 54     | 2.5    | 3.5   |      | V             | $V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table             |
|          |                                | 74     | 2.7    | 3.5   |      | V             |                                                                                                           |
| $V_{OL}$ | Output LOW Voltage             | 54, 74 |        | 0.25  | 0.4  | V             | $I_{OL} = 4.0 \text{ mA}$ , $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table |
|          |                                | 74     |        | 0.35  | 0.5  | V             | $I_{OL} = 8.0 \text{ mA}$ , $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table |
| $I_{IH}$ | Input HIGH Current             |        |        |       | 20   | $\mu\text{A}$ | $V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$                                                          |
|          |                                |        |        |       | 0.1  | mA            | $V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$                                                          |
| $I_{IL}$ | Input LOW Current              |        |        |       | -0.4 | mA            | $V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$                                                          |
| $I_{OS}$ | Short Circuit Current (Note 1) |        | -20    |       | -100 | mA            | $V_{CC} = \text{MAX}$                                                                                     |
| $I_{CC}$ | Power Supply Current           |        |        |       | 36   | mA            | $V_{CC} = \text{MAX}$                                                                                     |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

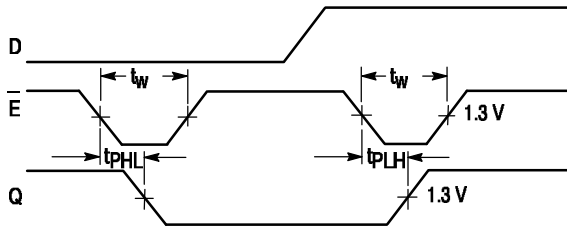
| Symbol    | Parameter                         |  | Limits |     |     | Unit | Test Conditions       |
|-----------|-----------------------------------|--|--------|-----|-----|------|-----------------------|
|           |                                   |  | Min    | Typ | Max |      |                       |
| $t_{PLH}$ | Turn-Off Delay, Enable to Output  |  |        | 22  | 35  | ns   | $C_L = 15 \text{ pF}$ |
| $t_{PHL}$ | Turn-On Delay, Enable to Output   |  |        | 15  | 24  | ns   |                       |
| $t_{PLH}$ | Turn-Off Delay, Data to Output    |  |        | 20  | 32  | ns   |                       |
| $t_{PHL}$ | Turn-On Delay, Data to Output     |  |        | 13  | 21  | ns   |                       |
| $t_{PLH}$ | Turn-Off Delay, Address to Output |  |        | 24  | 38  | ns   |                       |
| $t_{PHL}$ | Turn-On Delay, Address to Output  |  |        | 18  | 29  | ns   |                       |
| $t_{PHL}$ | Turn-On Delay, Clear to Output    |  |        | 17  | 27  | ns   |                       |

## AC SET-UP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

| Symbol | Parameter                    | Limits |     |     | Unit |
|--------|------------------------------|--------|-----|-----|------|
|        |                              | Min    | Typ | Max |      |
| $t_s$  | Input Setup Time             | 20     |     |     | ns   |
| $t_W$  | Pulse Width, Clear or Enable | 15     |     |     | ns   |
| $t_h$  | Hold Time, Data              | 5.0    |     |     | ns   |
| $t_h$  | Hold Time, Address           | 20     |     |     | ns   |

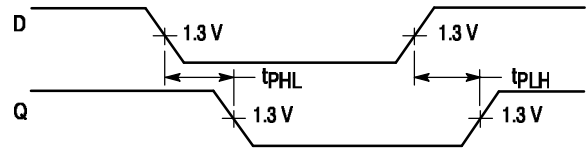
# SN54/74LS259

## AC WAVEFORMS



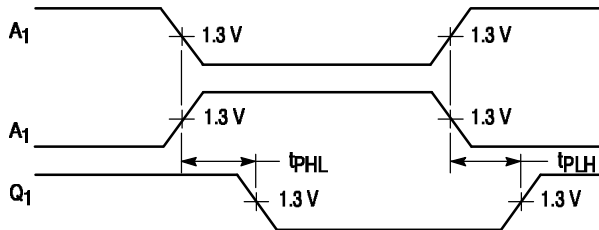
OTHER CONDITIONS:  $\bar{C} = H$ ,  $A = \text{STABLE}$

Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width



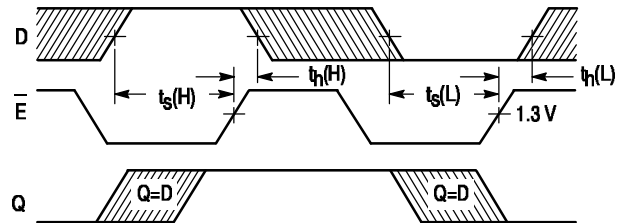
OTHER CONDITIONS:  $\bar{E} = L$ ,  $\bar{C} = H$ ,  $A = \text{STABLE}$

Figure 2. Turn-on and Turn-off Delays, Data to Output



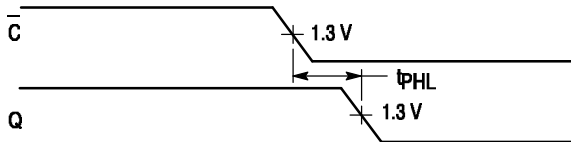
OTHER CONDITIONS:  $\bar{E} = L$ ,  $\bar{C} = L$ ,  $D = H$

Figure 3. Turn-on and Turn-off Delays, Address to Output



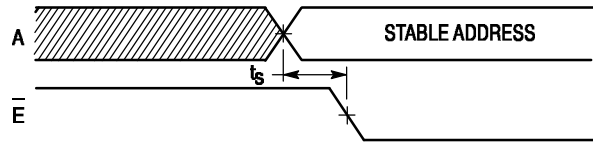
OTHER CONDITIONS:  $\bar{C} = H$ ,  $A = \text{STABLE}$

Figure 4. Setup and Hold Time, Data to Enable



OTHER CONDITIONS:  $\bar{E} = H$

Figure 5. Turn-on Delay, Clear to Output



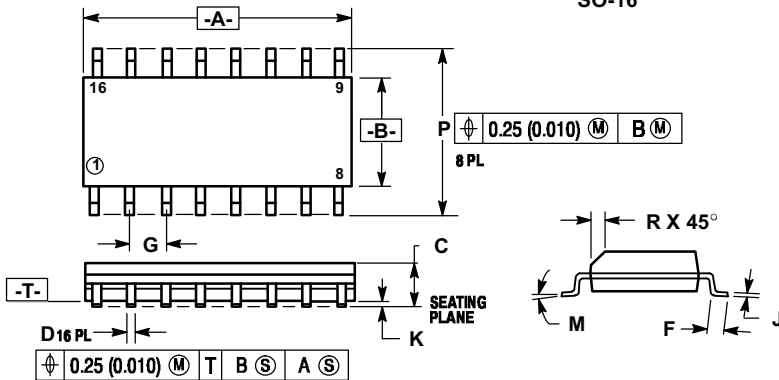
OTHER CONDITIONS:  $\bar{C} = H$

Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

### NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

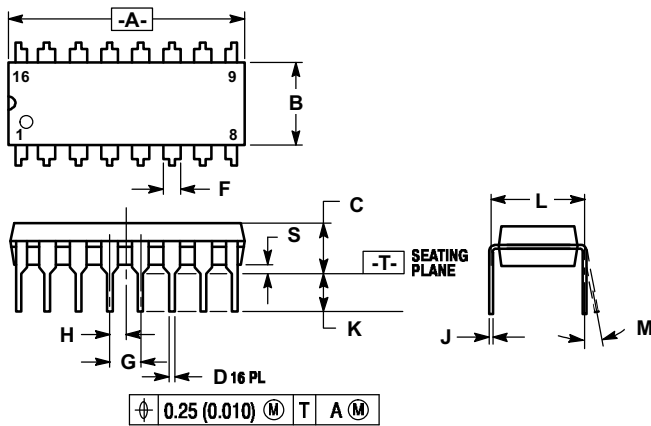
Case 751B-03 D Suffix  
16-Pin Plastic  
SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

| DIM | MILLIMETERS |           | INCHES |       |
|-----|-------------|-----------|--------|-------|
|     | MIN         | MAX       | MIN    | MAX   |
| A   | 9.80        | 10.00     | 0.386  | 0.393 |
| B   | 3.80        | 4.00      | 0.150  | 0.157 |
| C   | 1.35        | 1.75      | 0.054  | 0.068 |
| D   | 0.35        | 0.49      | 0.014  | 0.019 |
| F   | 0.40        | 1.25      | 0.016  | 0.049 |
| G   | 1.27 BSC    | 0.050 BSC |        |       |
| J   | 0.19        | 0.25      | 0.008  | 0.009 |
| K   | 0.10        | 0.25      | 0.004  | 0.009 |
| M   | 0°          | 7°        | 0°     | 7°    |
| P   | 5.80        | 6.20      | 0.229  | 0.244 |
| R   | 0.25        | 0.50      | 0.010  | 0.019 |

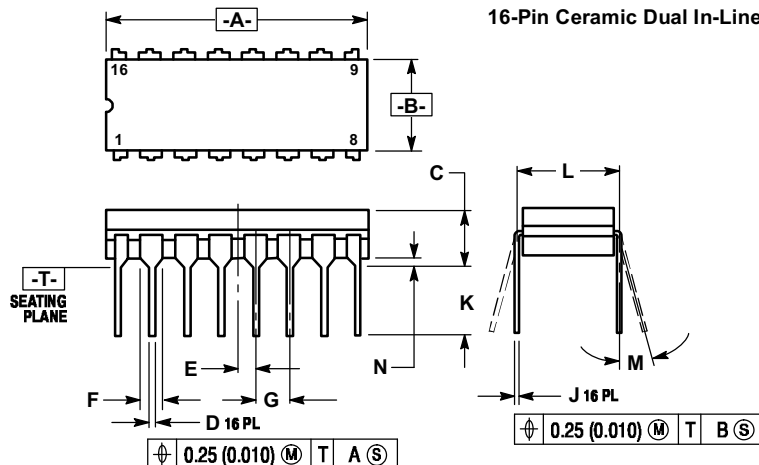
Case 648-08 N Suffix  
16-Pin Plastic



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

| DIM | MILLIMETERS |           | INCHES |       |
|-----|-------------|-----------|--------|-------|
|     | MIN         | MAX       | MIN    | MAX   |
| A   | 18.80       | 19.55     | 0.740  | 0.770 |
| B   | 6.35        | 6.85      | 0.250  | 0.270 |
| C   | 3.69        | 4.44      | 0.145  | 0.175 |
| D   | 0.39        | 0.53      | 0.015  | 0.021 |
| F   | 1.02        | 1.77      | 0.040  | 0.070 |
| G   | 2.54 BSC    | 0.100 BSC |        |       |
| H   | 1.27 BSC    | 0.050 BSC |        |       |
| J   | 0.21        | 0.38      | 0.008  | 0.015 |
| K   | 2.80        | 3.30      | 0.110  | 0.130 |
| L   | 7.50        | 7.74      | 0.295  | 0.305 |
| M   | 0°          | 10°       | 0°     | 10°   |
| S   | 0.51        | 1.01      | 0.020  | 0.040 |

Case 620-09 J Suffix  
16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

| DIM | MILLIMETERS |           | INCHES |       |
|-----|-------------|-----------|--------|-------|
|     | MIN         | MAX       | MIN    | MAX   |
| A   | 19.05       | 19.55     | 0.750  | 0.770 |
| B   | 6.10        | 7.36      | 0.240  | 0.290 |
| C   | —           | 4.19      | —      | 0.165 |
| D   | 0.39        | 0.53      | 0.015  | 0.021 |
| E   | 1.27 BSC    | 0.050 BSC |        |       |
| F   | 1.40        | 1.77      | 0.055  | 0.070 |
| G   | 2.54 BSC    | 0.100 BSC |        |       |
| J   | 0.23        | 0.27      | 0.009  | 0.011 |
| K   | —           | 5.08      | —      | 0.200 |
| L   | 7.62 BSC    | 0.300 BSC |        |       |
| M   | 0°          | 15°       | 0°     | 15°   |
| N   | 0.39        | 0.88      | 0.015  | 0.035 |

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